REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Official Action dated November 9, 2005. In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

Claims 1-3 are under consideration in this application. Claim 1 is being amended, as set forth in the above marked-up presentation of the claim amendments, in order to more particularly define and distinctly claim applicant's invention.

Additional Amendments

Claim 1 is being amended to correct formal errors and/or to better recite or describe the features of the present invention as claimed. All the amendments to the claims are supported by the specification. Applicant hereby submits that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

Claims 1-2 were rejected under 35 U.S.C. § 102(a)/102(e) on the grounds of being anticipated by US Pat. No. 6,339,560 to Naritake (hereinafter "Naritake"), and claim 3 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Naritake in view of US Pat. No. 5,506,808 to Yamada et al. (hereinafter "Yamada"). These rejections have been carefully considered, but are most respectfully traversed.

As now recited in claim 1, the read signal line (e.g., RIOT, RIOB in Figs. 1, 6) is different from said write signal line (e.g., WIOT, WIOB in Fig. 1) according to the invention. The write signal line WIOT, WIOB and said read signal line RIOT, RIOB are allocated crossing said sense amplifier column SA (e.g., 151, 153, 156, 158 in Fig. 15), while said write column selection line WS or WYS and said read column selection line RYS are allocated in parallel to said sense amplifier column 151, etc. The semiconductor memory device further includes a write buffer WB (in a box within the write buffer column 154 in Fig. 15) coupled to the write signal line WIOT, WIOB to output the write data ("*The write buffer column 154 is formed of a layout of a plurality of write buffers WB to drive the IO line*

for write based on the write data WD outputted from the input/output circuit 168." P. 13, 2nd paragraph), and a main amplifier MA (in a box within the main amplifier column 155 in Fig. 15) coupled **only** to the read signal line RIOT, RIOB to amplify the read data on the read signal line (Fig. 3; "*The main amplifier column 155 is formed of a layout of a plurality of main amplifier circuits MA to amplify the read data transferred to the read IO line from the bit line.*" P. 12, last paragraph). As shown in Fig. 15, the write data is transferred from the write buffer WB (to a sense amplifier circuit SA box then) to said bit line BL via the write signal line WIO, and the read data is transferred from said bit line BL (to a sense amplifier circuit SA box then) to said main amplifier MA via the read signal line RIO. As such, (1) the write data transmitted from the write buffer WB to the bit line and (2) the read data transmitted from the bit line to the main amplifier MA are transmitted via different paths WIO, RIO.

Applicants respectfully contend that the cited references fail to teach or suggest (1) "the write signal line WIOT, WIOB and said read signal line RIOT, RIOB crossing said sense amplifier column SA (e.g., 151, 153, 156, 158 in Fig. 15), while said write column selection line WS or WYS and said read column selection line RYS in parallel to said sense amplifier column 151 etc"; and (2) "a main amplifier MA (in a box within the main amplifier column 155 in Fig. 15) coupled **only** to the read signal line RIOT, RIOB to amplify the read data on the read signal line" according to the invention.

In contrast, Naritake's DL and DA (Fig. 2) are used for both read and write operations, such that Naritake does not disclose that the write signal line and the read signal line are separated.

In addition, Naritake's DL (Fig. 1) corresponds to the bit line BL of the invention, and Naritake's WCS corresponds to the write selection signal line WS or WYS of the invention, since the write selection signal line controls transmitting of the write data on the write signal line to the bit line BL. Naritake's WCS crosses the SA column, rather than extend in parallel to the SA column, as in the invention.

Even if, arguendo, assuming Naritake's WDL (Fig. 1) corresponds to the write signal line of the invention, Naritake's data amplifier DA 6 is coupled to both a read data line RDL and write data lines WDLn and /WDLn (Fig. 1), rather than only to the read data line RDL as the invention. As such, Naritake does not provide any main amplifier MA (in a box within the main amplifier column 155 in Fig. 15) coupled **only** to the read signal line RIOT, RIOB to amplify the read data on the read signal line as the invention. Naritake neither transfers the

read data from said bit line BL to such a main amplifier MA via the read signal line RIO which is different from the write signal line connecting between the write buffer WB and said bit line BL.

Yamada was relied upon by the Examiner to teach a sense amplifier circuit, but it does not compensate form the deficiencies as Naritake.

Applicant contends that neither Naritake, Yamada, nor their combination teaches or discloses each and every feature of the present invention as disclosed in independent claim 1. As such, the present invention as now claimed is distinguishable and thereby allowable over the rejections raised in the Office Action. The withdrawal of the outstanding prior art rejections is in order, and is respectfully solicited.

Conclusion

In view of all the above, clear and distinct differences as discussed exist between the present invention as now claimed and the prior art reference upon which the rejections in the Office Action rely, Applicant respectfully contends that the prior art references cannot anticipate the present invention or render the present invention obvious. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to contact the Applicant's undersigned representative at the address and telephone number indicated below.

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